PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Salman Akram

Serial No.: 09/829,161

Filed: April 9, 2001

For: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

Confirmation No.: 8260

Examiner: H. Nguyen

Group Art Unit: 2812

Attorney Docket No.: 2269-3442.1US (96-0428.01/US)

Notice of Allowance Mailed:

November 19, 2003

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EV326918120US

Date of Deposit with USPS: February 18, 2004

Person making Deposit: Christopher Haughton

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Title appear on page 3 of this paper.

Amendments to the Specification begin on page 4 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 7 of this paper.

Remarks begin on page 18 of this paper.

IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please enter the title as amended.

METHODS FOR MAKING METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS~~, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME~~

IN THE SPECIFICATION:

Please replace paragraph number **[0009]** with the following rewritten paragraph:

[0009] Several methods have been proposed to reduce stress notching. One proposed method uses a material less susceptible to stress notching, such as copper (Cu) or tungsten (W), in the conductive line. Using Cu in conductive lines, however, has in the past resulted in several problems. First, copper is difficult to etch. Second, adhesion between copper and adjacent insulating layers is poor and thus poses reliability concerns. Third, adding Cu to Al lines may reduce stress notching, but beyond a certain Cu concentration, device performance may begin to degrade. Fourth, as conductive line geometries shrink, adding Cu to Al lines seems less effective in reducing stress notching. Finally, even using Cu interconnects in the manner employed in the prior art can still lead to notching effects, especially at 0.1 μm geometries and below since, at such dimensions, line widths have become so small that any imperfection can cause ~~opens.~~ openings. Using W in Al conducting lines is also undesirable – W has a high resistivity and, therefore, reduces signal speed.

Please replace paragraph number **[0018]** with the following rewritten paragraph:

[0018] The present invention provides several advantages when compared to the prior art. One advantage is that ~~thermally-induced~~ thermally induced stress voids are reduced because the metal containing layer and metal containing spacer comprise materials exhibiting good thermal-voiding avoidance characteristics. Another advantage is that the size of conductive lines can be shrunk further in comparison to dimensions achievable by conventional processes, since only one additional deposition and etch step, without an additional masking step, is needed to form the metallization structure. Shrinking of conductive lines is necessary as device geometries decrease to less than 0.1 μm. At these small geometries, even small notches can significantly decrease conductivity.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] Metal containing layer 8 is deposited or otherwise formed by any process used in IC device fabrication. For example, metal containing layer 8 may be deposited by chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques, depending on the characteristics required of the layer. As used herein, the term "CVD techniques" encompasses, without limitation, plasma-enhanced CVD, or PECVD. Preferably, when metal containing layer 8 is Ti, this layer is formed by sputtering (a form of PVD) a film of Ti. If metal containing layer 8 is a metal nitride, it may be formed, for example, by depositing the metal in a ~~nitrogen-containing~~ nitrogen-containing atmosphere or by depositing the metal and annealing in a nitrogen-containing atmosphere. If-metal containing layer 8 is a metal silicide, it may be formed, for example, by first depositing either the metal containing layer or a silicon layer, then depositing the other, and heating to react the two layers and form the silicide. If metal containing layer 8 is a metal alloy, it may be formed by any process suitable for depositing the metal alloy. For example, either sputtering or CVD techniques can be employed.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] Conducting layer 10 is then formed over metal containing layer 8. Conducting layer 10 may comprise any conducting material used in IC device fabrication. Preferably, conducting layer 10 comprises a conducting metal, such as Al, optionally containing other elements such as Si, W, Ti, and/or Cu. More preferably, conducting layer 10 is an ~~aluminum-copper~~ aluminum-copper alloy. Conducting layer 10 may also be formed of Cu. Conducting layer 10 may be formed by any method used in IC device fabrication such as CVD or PVD techniques. Preferably, conducting layer 10 is deposited by a PVD method such as sputtering, as known in the art. Second dielectric layer 12 is next deposited or otherwise formed on top of conducting layer 10. Second dielectric layer 12 comprises any dielectric material used in IC device fabrication, including those listed above. Preferably, second dielectric layer 12 comprises a material that serves as an etch stop, as explained below. More preferably, second dielectric layer 12 comprises fluorine-doped silicon oxide or other low dielectric constant material. Second

dielectric layer 12 may be formed by any suitable process giving the desired physical and chemical characteristics, such as CVD, PECVD (plasma enhanced chemical vapor deposition), spin-on methods, or otherwise, depending upon the dielectric material selected. For use of the preferred fluorine-doped silicon oxide, the preferred deposition method is PECVD.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] The metallization structures illustrated in Figures 3a and 3b reduce ~~thermally-induced~~ thermally induced stress voids in conductive lines 100. Metal containing layer 8 and metal containing spacers 16 serve as a protective coating at the respective lower and lateral surfaces of conductive lines 100 and at intersections thereof, thereby reducing the incidence of stress voids by preventing them from starting at these surfaces and intersections thereof on conductive line 100. Metal containing layer 8 and metal containing spacers 16 also increase reliability of conductive line 100 without reducing its resistance.

Please replace paragraph number **[0052]** with the following rewritten paragraph:

[0052] Upper-metal containing layer 66 can be formed over conductive plug 64 in the following manner. Conducting layer 62 is deposited in aperture 56 and over dielectric layer 54 as described above with respect to Figure 5. Prior to completely filling aperture 56, however, the deposition of conducting layer 62 is halted as shown at 62a in Figure 5, leaving an upper portion of aperture 56 empty ~~(i.e,~~ (i.e., a recess is left at the top of aperture 56). Upper-metal containing layer 66 is then deposited over conducting layer 62, including the still-empty upper portion of aperture 56. Portions of conducting layer 62 and upper metal containing layer 66 above the horizontal plane of dielectric layer 54 are then removed by a planarization process, such as CMP, to form a completely enveloped, or clad, interconnect structure. If desired, portions of dielectric layer 54 and metal containing layer 52 flanking the interconnect structure can be removed as described above to form the structure of Figure 9.

IN THE CLAIMS:

Claims 27-71 and 83 were previously cancelled. None of the claims have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as previously amended.

Listing of Claims:

1. (Previously presented) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing barrier layer over the first dielectric layer;

forming a homogenous conducting layer directly on the at least one metal containing barrier layer;

forming a second dielectric layer in contact with the homogenous conducting layer;

removing aligned portions of the second dielectric layer, homogenous conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and

forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer.

2. (Previously presented) The method of claim 1, wherein said forming the first dielectric layer comprises forming a silicon oxide or BPSG layer.

3. (Previously presented) The method of claim 2, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

4. (Previously presented) The method of claim 3, further comprising forming a second metal containing barrier layer between a first metal containing barrier layer of said at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

5. (Previously presented) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride.

6. (Previously presented) The method of claim 1, wherein the at least one metal containing barrier layer is a single metal containing barrier layer and further comprising forming the single metal containing barrier layer of titanium or titanium nitride.

7. (Previously presented) The method of claim 1, wherein said forming the homogenous conducting layer comprises forming the homogenous conducting layer from at least one of aluminum and copper.

8. (Previously presented) The method of claim 7, wherein said forming the homogenous conducting layer comprises forming the homogenous conducting layer of an aluminum-copper alloy.

9. (Previously presented) The method of claim 1, wherein said forming the metal containing spacers comprises forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

10. (Previously presented) The method of claim 9, wherein said forming the metal containing spacers comprises forming the metal containing spacers of titanium or titanium nitride.

11. (Previously presented) The method of claim 1, wherein said forming a second dielectric layer comprises forming the second dielectric layer on the homogenous conducting layer to have sidewalls aligned with sidewalls of the homogenous conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer.

12. (Previously presented) The method of claim 11, further comprising forming the second dielectric layer of a low dielectric constant material.

13. (Previously presented) The method of claim 12, further comprising forming the second dielectric layer of a fluorine-doped silicon oxide.

14. (Previously presented) The method of claim 1, further comprising forming the at least one metal containing barrier layer and the metal containing spacers of a same metal.

15. (Previously presented) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

16. (Previously presented) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

17. (Previously presented) The method of claim 1, wherein said forming the homogenous conducting layer comprises forming the homogenous conducting layer by vapor deposition.

18. (Previously presented) The method of claim 17, further comprising forming the homogenous conducting layer by CVD, PVD or PECVD.

19. (Previously presented) The method of claim 1, wherein said forming the metal containing spacers comprises forming the metal containing spacers by vapor deposition and directional etching.

20. (Original) The method of claim 19, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

21. (Previously presented) The method of claim 1, wherein removing aligned portions of the second dielectric layer, homogenous conducting layer, and at least one metal containing barrier layer to form the multilayer structure is effected by patterning and etching the second dielectric layer, the homogenous conducting layer, and the at least one metal containing barrier layer.

22. (Previously presented) The method of claim 1, wherein said forming the metal containing spacers comprises forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

23. (Previously presented) The method of claim 22, wherein said forming the metal containing spacers comprises forming the metal containing spacer layer over the multilayer structure and first dielectric layer by a conformal deposition process.

24. (Previously presented) The method of claim 23, wherein portions of the metal containing spacer layer over the multilayer structure and first dielectric layer are removed by etching.

25. (Previously presented) The method of claim 1, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto to expose said homogenous conducting layer.

26. (Previously presented) The method of claim 25, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers by etching.

27.-71. (Canceled)

72. (Previously presented) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;

creating a homogenous conducting layer directly over the at least one metal containing barrier layer, said homogenous conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said homogenous conducting layer out of contact with any metal;

removing aligned portions of the homogenous conducting layer and at least one metal containing barrier layer to form a multilayer structure; and

flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer initiating at said at least one metal containing barrier layer and extending to substantially the same height as said homogenous conducting layer.

73. (Previously presented) The method of claim 72, further comprising forming a second dielectric layer in contact with said homogenous conducting layer.

74. (Previously presented) The method of claim 73, wherein said removing further comprises removing aligned portions of said second dielectric layer to form said multilayered structure.

75. (Previously presented) The method of claim 73, wherein said flanking at least one surface of the multilayer structure with a metal containing spacer comprises forming a metal containing spacer layer on said second dielectric layer.

76. (Previously presented) The method of claim 75, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

77. (Previously presented) The method of claim 76, wherein said removing any remaining portion is effected by etching.

78. (Previously presented) The method of claim 72, wherein said providing a substrate having a first dielectric layer comprises forming said first dielectric layer of a silicon oxide or BPSG layer.

79. (Previously presented) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

80. (Previously presented) The method of claim 79, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride.

81. (Previously presented) The method of claim 72, further comprising forming a second metal containing barrier layer between a first metal containing barrier layer of the at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

82. (Previously presented) The method of claim 72, wherein the at least one metal containing barrier layer is a single metal containing barrier layer and further comprising forming the single metal containing barrier layer of titanium or titanium nitride.

83. (Canceled)

84. (Previously presented) The method of claim 72, wherein said creating a homogenous conducting layer comprises creating the homogenous conducting layer of an aluminum-copper alloy.

85. (Previously presented) The method of claim 72, wherein said flanking comprises forming the metal containing spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

86. (Previously presented) The method of claim 85, wherein said forming the metal containing spacer comprises forming the metal containing spacers of titanium or titanium nitride.

87. (Previously presented) The method of claim 72, wherein said flanking at least one surface comprises forming said metal containing spacer on sidewalls of said multilayer structure.

88. (Previously presented) The method of claim 72, wherein said flanking at least one surface comprises forming said metal containing spacer on a top surface of said multilayer structure.

89. (Previously presented) The method of claim 72, further comprising forming a second dielectric layer on the homogenous conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal containing spacer to extend along the sidewalls of the second dielectric layer.

90. (Previously presented) The method of claim 89, wherein said forming the second dielectric layer comprises forming the second dielectric layer of a low dielectric constant material.

91. (Previously presented) The method of claim 90, wherein said forming the second dielectric layer comprises forming the second dielectric layer of a fluorine-doped silicon oxide.

92. (Previously presented) The method of claim 72, further comprising forming the at least one metal containing barrier layer and the metal containing spacer of a same metal.

93. (Previously presented) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

94. (Previously presented) The method of claim 93, wherein said forming the at least one metal containing barrier layer by vapor deposition comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

95. (Previously presented) The method of claim 72, wherein said creating a homogenous conducting layer comprises forming the homogenous conducting layer by vapor deposition.

96. (Previously presented) The method of claim 95, wherein said forming the homogenous conducting layer by vapor deposition comprises forming the homogenous conducting layer by CVD, PVD or PECVD.

97. (Previously presented) The method of claim 72, wherein said flanking comprises forming the metal containing spacer by vapor deposition and directional etching.

98. (Previously presented) The method of claim 97, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

99. (Previously presented) The method of claim 72, wherein removing aligned portions of the homogenous conducting layer and at least one metal containing barrier layer to form a multilayer structure is effected by patterning and etching the homogenous conducting layer and the at least one metal containing barrier layer.

100. (Previously presented) The method of claim 72, wherein said flanking comprises forming the metal containing spacer by forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first dielectric layer and a top portion of said multilayer structure.

101. (Previously presented) The method of claim 100, wherein said forming the metal containing spacer layer over the multilayer structure and first dielectric layer comprises forming the metal containing layer by a conformal deposition process.

102. (Previously presented) The method of claim 101, wherein said removing portions of the metal containing spacer layer is effected by etching.

103. (Previously presented) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing barrier layer over the first dielectric layer;

forming a homogenous conducting layer directly on the at least one metal containing barrier layer;

forming a second dielectric layer in contact with the homogenous conducting layer;

removing aligned portions of the second dielectric layer, the homogenous conducting layer, and the at least one metal containing barrier layer to form a multilayer structure;

forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers originating at said at least one metal containing barrier layer; and

removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto.

104. (Previously presented) The method of claim 103, wherein said removing any remaining portion is effected by etching.

105. (Previously presented) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;

creating a homogenous conducting layer directly on the at least one metal containing barrier layer;

forming a second dielectric layer on said homogenous conducting layer;

removing aligned portions of the second dielectric layer, the homogenous conducting layer and the at least one metal containing barrier layer to form a multilayer structure;

flanking at least one surface of the multilayer structure with a metal containing spacer such that said metal containing spacer originates at said at least one metal containing barrier and is substantially the same height as said second dielectric layer; and

removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

106. (Previously presented) The method of claim 105, wherein said removing any remaining portion is effected by etching.

REMARKS

This amendment corrects errors in the text. Entry is respectfully solicited.

Please note that claim 83 was canceled in applicant's amendment mailed to the Patent Office on May 16, 2003, but was included as an allowed claim in the Notice of Allowability. This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,

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Date: February 18, 2004
KWP/csw

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TRANSMITTAL LETTER

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant submits herewith Part B - Fee(s) Transmittal for the above-captioned application and a check in the amount of $1,645.00 in payment therefor plus five (5) copies of the patent when issued.

Also enclosed are Amendment Pursuant to 37 C.F.R. § 1.312(a); Comments on Statement of Reasons for Allowance; and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees.

Applicant understands that no additional fees are required. However, if the Office determines that any comparison fees or other additional fees are required, the Commissioner is authorized to charge any such fees to TraskBritt Deposit Account No. 20-1469. A copy of this Transmittal Letter is enclosed for deposit account charging purposes.

Respectfully submitted,

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Date: February 18, 2004
KWP/dlm:ljb
Enclosures: Part B - Issue Fee Transmittal
Check No. 19902 in the amount of $1,645.00
Copy of Transmittal Letter
Amendment Pursuant to 37 C.F.R. § 1.312(a) (18 pages)
Comments on Statement of Reasons for Allowance (2 pages)
Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages)

Document in ProLaw

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NOTICE OF EXPRESS MAILING

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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
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PO Box 1450
Alexandria, VA 22313-1450

Sir:

The Examiner indicates in the April 25, 2003 office action:

> Claims 25 and 76 recite the features removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto. These features in combination with the other elements of the claims are neither disclosed nor suggested by the prior art of record. Claims 26 and 77 depend from claim 25 or 76, they are allowed for the same reason.

Applicant concurs with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. However, claims 25, 26, 76 and 77 include other and different language than that specified by the Examiner. Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Respectfully submitted,

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